What is claimed is:

1) A circuit, comprising:

a first digital to analog converter ("DAC") to generate a first current;

a first transistor, coupled to the first DAC, to generate a first biasing current responsive to the first current; and,

a second DAC, coupled to the first transistor, to generate a first control current responsive to the first biasing current.

2) The circuit of claim 1, wherein the first DAC is a binary weighted control DAC.

3) The circuit of claim 2, wherein the second DAC is a binary weighted control DAC.

4) The circuit of claim 3, wherein binary weighted values of the second DAC is obtained in response to a calibration signal generated by a controller.

5) The circuit of claim 3, wherein the first DAC is an M-bit DAC and the second DAC is an N-bit DAC, wherein M is less than N.

6) The circuit of claim 1, wherein the second DAC is a current source.

7) The circuit of claim 1, wherein the second DAC is coupled to a pin.

8) The circuit of claim 1, wherein the first transistor is a p-type transistor.

9) The circuit of claim 1, wherein the binary weighted values are stored in a register.

10) The circuit of claim 1, wherein the circuit is in a memory device.

11) The circuit of claim 1, further comprising:

a second transistor, coupled to the first DAC, to generate a second biasing current responsive to the first current; and,

a third DAC, coupled to the second transistor, to generate a second control current responsive to the second biasing current.

12) A current distribution circuit in a memory device, comprising:

a first M-bit digital-to-analog converter ("DAC") to generate a first current;

a first transistor, coupled to the first M-bit DAC, to generate a first biasing current responsive to the first current;

a second N-bit DAC, coupled to the first transistor, to generate a first control current responsive to the first biasing current;

a second transistor, coupled to the first M-bit DAC, generating a second biasing current responsive to the first current; and,

a third N-bit DAC, coupled to the second transistor, to generate a second control current responsive to the second biasing current.

13) The circuit of claim 12, wherein M is less than N.

14) The circuit of claim 12, wherein the memory device is a dynamic random access memory ("DRAM") device.

15) The circuit of claim 12, wherein the first and the second transistors are p-type transistors.

16) The circuit of claim 12, wherein the second DAC is coupled to a first pin and the third DAC is coupled to a second pin.

17) The circuit of claim 12, wherein N values for the second and third N-bit DAC are obtained in response to a calibration signal generated by a controller.

18) An apparatus for calibrating an output driver, comprising:

a controller to generate a calibration signal; and,

a device, coupled to the controller, to generate an output signal in response to the calibration signal, wherein the device includes a circuit having:

a first M-bit digital-to-analog converter ("DAC") to generate a first current;

a first transistor, coupled to the first M-bit DAC, to generate a first biasing current responsive to the first current;

a second N-bit DAC, coupled to the first transistor, to generate a first control current responsive to the first biasing current;

a second transistor, coupled to the first M-bit DAC, generating a second biasing current responsive to the first current; and,

a third N-bit DAC, coupled to the second transistor, to generate a second control current responsive to the second biasing current.

19) The apparatus of claim 18, wherein M is less than N.

20) The apparatus of claim 18, wherein the device is a Rambus dynamic random access memory ("RDRAM") device.

21) The apparatus of claim 18, wherein the controller is a memory controller.

22) The apparatus of claim 18, wherein the first and the second transistors are p-type transistors.

23) The apparatus of claim 12, wherein the second DAC is coupled to a first pin and the third DAC is coupled to a second pin, and wherein the first and second pins are coupled to the controller.

24) A method for calibrating an output driver, comprising the steps of:

providing m values to a M-bit DAC to generate a first current;

providing a first biasing current, in response to the first current, to a N-bit DAC coupled to the output driver;

obtaining the m most significant bit values of the N-bit DAC;

applying the m most significant bits to the M-bit DAC to generate a second current;

providing a second biasing current, in response to the second current, to the N-bit DAC; and,

obtaining a control current for the output driver in response to the second biasing current.